REMARKS

Claims 10-15 are pending in the present application. Claims 1-9 have been canceled. Claims 10-15 have been presented herewith.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119 and receipt of the certified copy of the priority document.

Information Disclosure Statement

Enclosed is a copy of an Information Disclosure Statement and form PTO-1449 filed along with the present application on November 30, 2001. Also enclosed is a dated, stamped postcard receipt provided as evidence that the Information Disclosure Statement was received by the U.S. Patent Office. Applicant notes that Japanese Patent publication No. 11-233632 was submitted along with the Information Disclosure Statement as including an English language abstract, and is described in the "RELATED ART" section beginning on page 1 of the present application. **The Examiner is respectfully requested to acknowledge receipt of the Information Disclosure Statement, and to confirm on the record that the Japanese Patent publication has been considered and will be cited of record in the present application.**

Claim Rejections-35 U.S.C. 112

Claims 1-5 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. As noted above, claims 1-5 have been canceled. Applicant respectfully submits that pending claims 10-15 are in compliance with 35 U.S.C. 112, second paragraph. Applicant therefore respectfully requests withdrawal of this rejection insofar as it may pertain to the presently pending claims.

Claim Rejections-35 U.S.C. 103

Claims 1-9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Tahara et al. reference (U.S. Patent No. 5,356,515) in view of the Yamada reference (U.S. Patent No. 5,827,778). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The method of forming a conductive path in a semiconductor device of claim 10 includes in combination "etching a hole in the insulating layer to the conductive member using the etching mask and a reactive gas, the hole including a misalignment groove in the insulating layer at a side of the conductive member that corresponds to the offset portion of the opening in the etching mask"; and "stopping a downward extension of said etching of the misalignment groove by using a polymeric product as an etch stop, the polymeric product generated by a polymeric film generating action of the reactive gas during said etching". Applicant respectfully submits that the prior art as relied upon by the Examiner does not disclose or make obvious these features.

The Examiner has asserted that the Tahara et al. reference shows various process conditions, and that the Tahara et al. reference also states that various etching conditions in addition to the conditions specified may be used (column 17, lines 13-30). However, the Tahara et al. reference as relied upon by the Examiner does not disclose or suggest selecting particular etch conditions so as to stop etching of a misalignment groove by using a polymeric product as an etch stop, the polymeric product being generated by polymeric film generating action of reactive gas during etching. The Tahara et al. reference also does not appear to disclose misalignment grooves.

The Examiner has relied upon the Yamada reference as showing a CHF_3/CO flow rate of 15/85. However, the Yamada reference also fails to disclose or suggest selecting particular etch conditions so as to stop etching of a misalignment groove by using a polymeric product as an etch stop, the polymeric product being generated by polymeric film generating action of reactive gas during etching.

On page 4 of the Office Action dated April 7, 2003, the Examiner has alleged that it is well known that the etching process of using carbon-containing etchant gas produces polymeric byproducts which deposit on the sidewalls and bottom of a hole. The Examiner has offered the Pu et al. reference (U.S. Patent No. 5,843,847) as evidence thereof. However, although the generating and depositing of polymeric byproducts during etching may be known, the prior art as relied upon by the Examiner (including the Pu et al. reference offered as evidence by the Examiner), does not specifically disclose or suggest using the polymeric byproducts as an etch stop to

prevent further etching of a misalignment groove. In absence of such specific and particular teaching in the relied upon prior art, Applicant respectfully submits that this rejection is based on impermissible hindsight. Accordingly, Applicant respectfully submits that the method of forming a conductive path of claim 10 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 10-15, is improper for at least these reasons.

Applicant also respectfully emphasizes that the Tahara et al. reference as relied upon by the Examiner discloses etching of **silicon dioxide** layer 82, as described beginning in column 12, line 52. In contrast, the Yawada reference as relied upon by the Examiner discloses etching of **silicon oxide film 14 and silicon flouride oxide film 15**, as described beginning in column 7, line 27 with respect to Figs. 5 and 6, not etching of a silicon dioxide in particular. Since the references do not disclose etching of a same material, Applicant respectfully submits that the teachings are incompatible. Accordingly, Applicant respectfully submits that the method of forming a conductive path of claim 10 would not have been obvious in view of the prior art as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 10-15, is improper for at least these additional reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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Enclosures: Version with Marked-Up Changes
Copy of Information Disclosure Statement, 1449 Form
Japanese Patent Publication
Copy of postcard receipt

VERSION WITH MARKED-UP CHANGES

Additions/Deletions to the Abstract:

A method for manufacturing a semiconductor device [(18)] including a conductive path [(32a)] extending from the upper surface of an insulating layer [(23)] on a semiconductor substrate [(22)] to a conductive member [(24)] embedded in the insulating layer [(23)]. An etching mask [(26)], which defines an etched hole [(27)] for the conductor path, is formed on the insulating layer [(23)] within a specified permissible error, and that portion of the insulating layer [(23)] which is not covered by the etching mask [(26)] is removed by a reactive ion etching unit [(10)] having a reaction chamber [(11)] into which a reactive gas of CHF_3/CO is introduced at a CHF_3/CO flow ratio of about 15/85. After this, the etched hole [(27)] formed by an etching process is filled with a conductive material [(32)] for the conductive path [(32a)].

Additions/Deletions to the Specification:

Page 7, lines 16-18:

In the example shown in Fig. 1(a), in the insulating layer 23, a second conductive member 25 is embedded as a lower electrode member below the electrode member 24.

Page 7, line 26 through to page 8, line 6:

In the resist mask 26, an opening 26a is formed with a diameter D1 of [0.2~0.3m] 0.2~0.3μm, for example, which substantially corresponds to the width of the

electrode member 24. The reactive ion etching unit 10 is used to remove a region of the insulating layer 23 exposed through the opening 26a to thereby form an etched hole 27 leading to the electrode member 24. For a selective etching process to form the etched hole 27, the semiconductor device is placed on the sample holder 19 such that the surface 23a of the insulating layer 23 faces the upper electrode 15 of the reactive ion etching unit 10.

Page 9, line 25 through to page 10, line 2:

The etching stop phenomenon was [not] observed during a one-minute etching process at a point indicated by a code 28a on the characteristic curve 28 and at a point indicated by a code 29a on the characteristic curve 29, but the etching stop phenomenon did not take place at any other points on the other characteristic curves [curve].

Page 10, lines 18-20:

Referring back to Fig. 1(c) [Fig. 2(c)], a distance H from the upper surface of the electrode member 24 to the lower electrode member 25 is generally larger than 300nm.

Page 10, line 21 through to page 11, line 2:

Therefore, if the permissible placement error of the resist mask 26 is limited to 0.04μm and the resist mask 26 is placed properly within this error limit, by performing the etching process to the insulating layer 23 under the condition that the reaction

chamber pressure is maintained at 100mTorr or higher while supplying the reaction chamber 11 of the reactive ion etching unit 10 with a mixed reaction gas of CHF_3 and CO at a flow ratio of about 15/85 for these component gases, as shown in [Fig. 2(c)] Fig. 1(c), the unaligned portion due to the offset s of the etched hole 27 never reaches the lower electrode member 25 even if there is an offset within the permissible error.

Page 11, lines 17-21:

Fig. 4 is a graph (2) obtained from results of an experiment to find the etching stop condition, in which, as in the graph (1) of Fig. 3, the horizontal axis denotes offsets s (in μm) of the resist mask 26 and the vertical axis denotes depths d (in [μm] nm) (see Fig. 1(c)) of the unaligned portion of the etched hole 27 from the upper surface of the electrode member 24 by etching for one minute.

REQUEST FOR EARLY NOTIFICATION OF SERIAL NUMBER

ATTY DOCKET #: OKI.286 **DUE DATE:** August 21, 2002

APPLICANT: Naokatsu IKEGAMI

SERIAL NO.: (NEW) **FILING DATE:** November 30, 2001

TITLE: METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE

RECEIPT OF THE FOLLOWING PAPERS IS ACKNOWLEDGED:
New U.S. Patent Application including: Utility Patent Application Transmittal; Recordation Form Cover Sheet including Assignment (2 pages); specification, claims and abstract (17 pages); Declaration and Power of Attorney (3 pages); 5 sheets of drawings for Figures 1-4; Claim of Priority including certified priority document; Transmittal of Information Disclosure Statement, PTO-1449 Form and 1 reference; and $780 filing fee.

DATE: November 27, 2001 **ATTY:** ACV **[Check No. 9235]**